UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/637,049	08/11/2000	Fan Zhou	FORE-67	7201

7590 03/11/2004

EXAMINER
MOORE, IAN N

ART UNIT	PAPER NUMBER
2661	7

Ansel M. Schwartz
One Sterling Plaza
Suite 304
201 N. Craig Street
Pittsburgh, PA 15213

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/637,049	ZHOU ET AL.	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This is in response to amendment filed on February 13, 2004 (paper # 6).

Claim Objections

2. Currently amended Claim 5 is objected to because of the following informalities: claim 5 recites, "... the port card assembling the packet **from** the stripes of the fragments of the packets **the port card receives from the fabrics**." It is unclear what is being assembled and what is being received. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros (U.S. 5,166,926) and Gaddis (U.S. 5,815,501), and further in view of Koehler (U.S. 6,650,660).

Regarding claim 1, Cisneros '926 discloses a switch for switching packets, each packet having a length, comprising:

a port card (see FIG. 3A, Interface Module 210) which receives packets from (see Fig. 3A Incoming User Lines 305) and sends packets to a network (Fig. 3A Outgoing User

lines 335; see col. 15, line 44-65, note that each Interface module transmits and receives cells); and

fabrics connected to the port card which switch the packets (see Cisneros '926 Fig. 5, Self-routing cross-point planes 550s connects to Interface Modules 260 and 270; and col. 25, line 63 to col. 26, line 27; Note that Self-routing cross-point planes 550s are "fabrics") and the port card sending packets to the fabrics (see FIG. 5, Each Input side of Interface Module $260_{1\text{-}k}$ sends cells to Self-routing cross-point planes).

Cisneros '926 does not explicitly disclose a fabric (see Gaddis '501 FIG. 3, the ATM ATM Ethernet portal Hardware) having a memory mechanism (see Gaddis '501 FIG.3, a combined functionality of Dual-ported Share Memory 24, Control Microprocessor 20, DMA Controller 26 and ATM cell processor), and a fabric having a mechanism for determining the length of each packet (see Gaddis '501 Fig. 5, a length of the arriving Ethernet Frame) received by the fabric and placing a length indicator with the packet (see Gaddis '501 Fig. 5, putting a value in a "SIZE" field in the ATM encapsulation; see col. 8, line 1-17; note that a size field indicates the number of bytes in segment data field. By utilizing the last segment's size field and sequence number, a variable Ethernet frame/packet size is defined.) so when the packet is stored in the memory mechanism, the determining mechanism can identify from the length indicator how long the packet is and where the packet ends in the memory mechanism (see Gaddis '501 col. 9, line 9-46; note the shared memory places the frames into the memory. Each segment is 44 bytes long, except the last segment. In the shared memory, each 44 byte segments are stored, and the gaps between each segments are padded with inter-cell padding as the placeholders for ATM and SAR headers. Therefore, in order to determine

the beginning and the end of each Ethernet frame and being able to insert the placeholders for ATM headers, the shared memory must have a functionally to locate/identify each frame by its size (i.e. the start of the frame or the end of the frame); also see col. 6, line 61-64) .

However, this limitation is taught by Gaddis '501. Cisneros '926 teaches the interface card, which transmits and receives cells and a cross connect plane switch. Gaddis '501 teaches frame segmentation and storing into a shared memory, which locates each frame by the size. Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the purpose of dramatically decreasing the processing required by the portal and increasing the data throughput rate. The motivation being that by designing a portal unit switch between Ethernet and ATM system, it will decrease the protocol converting time since the ATM network connection can be setup transparently between Ethernet segments.

Neither Cisneros '926 nor Gaddis '501 explicitly discloses sending strips of corresponding fragments of each packet.

However, the above-mentioned claimed limitations are taught by Koehler'660. In particular, Koehler'660 teaches sending strips of corresponding fragments of each packet (see FIG.1 Splitting Circuitry 16) to the fabrics (see FIG.1 Functional Circuits 26 and 28; see col. 5, line 4-52; note that each 32-bits packet is splitted/stripped into two 16 bits portions and transfer along two respective parallel switch/fabric/circuit paths. Thus, it is clear that a stripped/splitted of portion/fragment of a packet is send to Functional switch/fabric circuit 26, and its corresponding/associated stripped/splitted of portion/fragment of a packet is send to Functional switch/fabric circuit 28).

In view of this, having the combined system of Cisneros '926 and Gaddis '501, then given the teaching of Koehler'660, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Cisneros '926 and Gaddis '501, by providing the interface card (of Cisneros '926) with feature of splitting and sending portions/fragments of packet to its respective switching circuits, as taught by Koehler'660, for the purpose of increasing efficiency of packet switching by implementing multiple small devices to operate in parallel, rather than utilizing a single large device (see Koehler'660 col. 1, lines 14-26). The motivation being that by splitting the packet into fragments and processing each portion/fragment in parallel, it will increase the processing speed, reduce the processing time, and decrease the cost to build large circuit/switch device.

Regarding claim 2, Koehler'660 teaches receiving the strips of the packets as described above in claim 1. Gaddis '501 discloses the determining mechanism includes an aggregator (see Gaddis '501 Fig. 3 Ethernet Controller 22 at the transmission side (i.e. Ethernet to ATM path)) which receives packet fragments from the port card (see Gaddis '501 Fig. 3 Ethernet Controller 22 receiving frame segments from Serial Interface Adapter 22), determines the packet length and appends packet length information to the beginning of the packet in the length indicator (see Gaddis '501 Fig. 5, note that in the ATM encapsulation, a "SIZE" field is attached to the header with the value, which indicates the number of bytes in segment data field; also see col. 8, line 1-17, by utilizing the last segment's size field and sequence number, a variable size Ethernet frame/packet is computed/defined.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 and Gaddis '501 as taught by Koehler'660 for the same reason stated in Claim 1 above.

Regarding claim 3, Gaddis '501 discloses the memory mechanism includes a memory controller (see Gaddis '501 FIG.3, a combined system of Dual-ported Share Memory 24, the Control Microprocessor 20, ATM cell processor and DMA Controller), the aggregator (see Gaddis '501 Fig. 3 Ethernet Controller 22) sending the packet with the packet length information to the memory controller (see Gaddis '501 col. 5, line 25-33) which stores the packet with the packet length information (see Gaddis '501 col. 5, line 54-60 and col. 9, line 9-46). Note that Ethernet frames with the size/length fields are send from Ethernet Controller to the shared Memory, and the formatted Ethernet frames are stored in the shared memory.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 and Gaddis '501 as taught by Koehler'660 for the same reason stated in Claim 1 above.

4. Claims 4-6 rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros '926, Gaddis '501 and Koehler'660, as applied to claims 1-3 above, and further in view of Joffe (U.S. 6,021,086).

Regarding claim 4, Gaddis '501 discloses that the memory controller has a memory as described in Claim 1-3 above.

Neither Cisneros '926 nor Gaddis '501 explicitly discloses a memory which has a wide cache buffer structure in which multiple packets are put into one word (see Joffe '086 Fig. 5, Shared Memory 26, bits from multiple ports (B1, B2) (i.e. note that multiple ports transmit/receive multiple packets), and Words (W1-Wn); see col. 5, line 46-67; note that one bit from each port is responsible for a single bit position in each word stored in the shared memory. When pluralities of packets arrive at a port, each bit is transferred and stored into each word at the shared memory (i.e. Bit 1 to Bit m storing in each W1 to Wn).)

However, this limitation is taught by Joffe '086. Note that Joffe '086's shared buffer memory has a functionality of storing bits from various packets into a single word. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Cisneros '926 and Gaddis '501, as taught by Joffe '086, for the purpose of designing an improved architecture for providing multiple port access to store multiple packets to a shared memory; see Joffe '086 col. 3, line 1-3. The motivation being that by designing a shared memory buffer which stores each bit from plurality of packets into a single word, it can reduce extra space in the shared buffer memory.

Regarding claim 5, the combined system of Cisneros '926, Gaddis '501, Koehler'660 and Joffe '086 discloses that the fabric sends/receives the strips of fragments of the packet to/from the port card as described above in Claim 1-4. Gaddis '501 further discloses the fabric includes a separator (see Gaddis '501 Fig. 3 Ethernet Controller 22 at the receiving side (i.e. ATM to Ethernet path)) which reads the packets from the memory controller and

extracts the packet length information from each packet to determine when each packet ends (see Gaddis '501 Fig. 10; and col. 10, line 1-40; note that when ATM cells arrive from the network, the microprocessor examines each cell to ensure all ATM cells that belongs to an Ethernet frame are received by utilizing the frame size and frame size counter. Once an entire Ethernet frame arrives, Ethernet controller extracts the segments from the shared memory, and then reassembles the Ethernet frame. When the segment is extracted, the size is also extracted from the memory since the size field is in the header of the cells. In order to reassemble Ethernet frame from the ATM cells, the controller must identify where the frame ends.) Moreover, Koehler'660 discloses assembling the packet from the strips of the fragments of the packet receives from the fabrics (see FIG. 1, Grouping Circuitry 38; see col. 6, lines 6-65; note that the grouping circuitry reassembles/groups the splitted portions of each packet from the Functions circuits/switches/fabrics back into an original packet.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Cisneros '926, Gaddis '501, and Koehler'660, as taught by Joffe '086 for the same reason stated in Claim 4 above.

Regarding claim 6, Cisneros '926 disclose a fabric sending any fragments of each packet to an unstriper of the port card (see FIG. 3A, De-multiplexer 330 of the Interface Module 210 is an "unstriper of the port card"; see col. 16, line 26-48; note that various parts of the cells, from the cross connect plane, are received at the de-multiplexer.) Gaddis '501 discloses that the separator removes the packet length information from each packet before sending any fragments (see Fig. 10; Fig. 5 Ethernet frame and ATM cell, and col. 10, line 31-

58; note that each time a new ATM cell is arrived, the size field is updated, which means that the current size of the frame must be deleted first in order to be updated. Once all ATM cells that belong to an Ethernet frame arrive, an Ethernet frame is reconstructed as shown in Fig, 5, an Ethernet frame without SIZE field. Thus, it is clear that the size field is deleted after reassembly process at the Ethernet Controller).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Cisneros '926 and Gaddis '501as taught by Joffe '086 for the same reason stated in Claim 4 above.

5. Claims 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros (U.S. 5,166,926) in view of Gaddis (U.S. 5,815,501).

Regarding claim 7, Cisneros '926 discloses a method for switching packets having a length comprising the steps of:

receiving a packet at a port card of a switch (see FIG. 3A, Interface Module 210 and Incoming User Lines 305; see col. 15, line 44-65, note that each Interface module receives the user packets);

sending fragments of the packet to fabrics of the switch and receiving the fragments of the packet at the fabrics of the switch from the port card (see Cisneros '926 Fig. 5, Self-routing cross-point planes 550s connects to Interface Modules 260 and 270; and col. 25, line 63 to col. 26, line 27; Note that the self-routing cross-point planes 550s are "the fabrics of the switch". Since each ATM cell has a fixed size format, it must carry fixed size segments of the variable size user packet. Moreover, the cross-point planes are the switch matrixes, which route the ATM cells to/from the same/different user packet into various paths within the

matrix. Thus, the segments of the user packet are transmitted/received between the Interface Units and cross connect planes. Also, each Input side of Interface Module 260_{1-k} sends cells to Self-routing cross-point planes).

Cisneros '926 does not explicitly disclose measuring the length of the packet at each fabric (see Gaddis '501 FIG. 3, the ATM Ethernet portal Hardware) from the fragments of the packet received at the fabric (see Gaddis '501 col. 7, line 39-48, note that since SAR protocol is used to segment the Ethernet frame, it must first determine the size of the Ethernet frame.);

appending a length indicator to the packet (see Gaddis '501 Fig. 5, putting a value in a "SIZE" field in the ATM encapsulation; see col. 8, line 1-17; note that a size field indicates the number of bytes in segment data field. By utilizing the last segment's size field and sequence number, a variable Ethernet frame/packet size is defined);

storing the packet with the length indicator in a memory mechanism of the fabric (see Gaddis '501 Fig. 3, the functionality of dual shared memory 24, control microprocessor 20, DMA controller 26 and ATM cell processor is the "memory mechanism"; col. 9, line 9-46; note that the shared memory places the frames into the memory. Each segment is 44 bytes long, except the last segment. In the shared memory, each 44 byte segments are stored, and the gaps between each segments are padded with inter-cell padding as the placeholders for ATM and SAR headers. Therefore, in order to insert the placeholders for ATM headers, the shared memory must have a functionally to determine the beginning and the end of each frame and being able to locate/identify each frame by its size (i.e. the start of the frame or the end of the frame). Also see col. 6, line 61-64);

reading the packet from the memory mechanism (see Gaddis '501 Fig. 9 and col. 10, line 1-40; note that Ethernet Controller reads each segment from the memory in order to reassemble the frame. Also see col. 6, line 61-64); and

determining where the packet ends from the length indicator of the packet (see Gaddis '501 col. 10, line 1-40; note that when ATM cells arrive from the network, the microprocessor examines to ensure all ATM cells, that belong to an Ethernet frame, are received by utilizing the frame size and frame size counter. Once an entire Ethernet frame arrives, Ethernet controller reassembles the Ethernet frame from the segments. In order to reassemble Ethernet frame from the ATM cells, the controller must identify where the frame ends.)

However, this limitation is taught by Gaddis '501. Cisneros '926 teaches the interface card, which receives cells from the network and transmits to the cross connect planes. Gaddis '501 teaches a frame segmentation process that utilizes the size/length of the Ethernet frame to form an ATM cell, storing process that utilizes a shared memory, and re-assembly process that utilizes the size/length of the Ethernet frame. Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the purpose of dramatically decreasing the processing required by the portal and increasing the data throughput rate. The motivation being that by designing a portal unit switch between Ethernet and ATM system, it will decrease the protocol converting time since the ATM network connection can be setup transparently between Ethernet segments.

Neither Cisneros '926 nor Gaddis '501 explicitly discloses sending/receiving corresponding fragments of the packet as stripes.

However, the above-mentioned claimed limitations are taught by Koehler'660. In particular, Koehler'660 teaches sending/receiving corresponding fragments of the packet as stripes (see FIG.1 Splitting Circuitry 16) to the fabrics (see FIG.1 Functional Circuits 26 and 28; see col. 5, line 4-52; note that each 32-bits packet is splitted/stripped into two 16 bits portions and transfer along two respective parallel switch/fabric/circuit paths. Thus, it is clear that a stripped/splitted of portion/fragment of a packet is send to Functional switch/fabric circuit 26, and its corresponding/associated stripped/splitted of portion/fragment of a packet is send to Functional switch/fabric circuit 28. Also, note that each splitted portion of the packets is received at Functional Circuits 26 and 28.)

In view of this, having the combined system of Cisneros '926 and Gaddis '501, then given the teaching of Koehler'660, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Cisneros '926 and Gaddis '501, by providing the interface card (of Cisneros '926) with feature of splitting and sending portions/fragments of packet to its respective switching circuits, as taught by Koehler'660, for the purpose of increasing efficiency of packet switching by implementing multiple small devices to operate in parallel, rather than utilizing a single large device (see Koehler'660 col. 1, lines 14-26). The motivation being that by splitting the packet into fragments and processing each portion/fragment in parallel, it will increase the processing speed, reduce the processing time, and decrease the cost to build large circuit/switch device.

Regarding claim 8, the combined system of Cisneros '926, Gaddis '501 and Koehler'660 discloses the fabrics. Gaddis '501 discloses the step of receiving fragments at an aggregator of the fabric (see Gaddis '501 Fig. 3 Ethernet Controller 22 at the transmission side (i.e. Ethernet to ATM path) is the "aggregator", and it receives Ethernet segments via Serial Interface). Thus, each fabric in the combined system of Cisneros '926, Gaddis '501 and Koehler'660 can further be modified to have an aggregator per Gaddis '501 teaching.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 and Gaddis '501 as taught by Koehler'660 for the same reason stated in Claim 7 above.

Regarding claim 9, Gaddis '501 discloses the step of measuring the length of the packet with the aggregator (see Gaddis '501 col. 7, line 39-48, note that since SAR protocol is used to segment the Ethernet frame, it must first determine the size of the Ethernet frame. Also, see col. 8, line 1-17, by utilizing the last segment's size field and sequence number, a variable size Ethernet frame/packet is computed/defined.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 and Gaddis '501 as taught by Koehler'660 for the same reason stated in Claim 7 above.

Regarding claim 10, Gaddis '501 discloses the step of the appending the length indicator to the packet with the aggregator (see Gaddis '501 Fig. 5, note that in the ATM

encapsulation, a "SIZE" field is attached to the header with the value, which indicates the number of bytes in segment data field.).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 and Gaddis '501 as taught by Koehler'660 for the same reason stated in Claim 7 above.

Regarding claim 11, Gaddis '501 discloses the step of storing the packet with the length indicator in a memory controller of the memory mechanism (see Gaddis '501 FIG.3, a combined system of Dual-ported Share Memory 24, the Control Microprocessor 20, ATM cell processor, and DMA Controller is "a memory controller"; see col. 5, line 54-60 and col. 9, line 9-46). Note that Ethernet frames with the size fields are send from Ethernet Controller to Shared Memory, and the formatted Ethernet frames are stored in the shared memory.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 and Gaddis '501 as taught by Koehler'660 for the same reason stated in Claim 7 above.

Regarding claim 12, Gaddis '501 discloses the step of reading the packet from the memory controller with a separator of the fabric (see Gaddis '501 Fig. 3 Ethernet Controller 22 at the receiving side (i.e. ATM to Ethernet path) is "a separator"; also see Gaddis '501 Fig. 9 and col. 10, line 1-40; note that Ethernet Controller reads each segment from the memory in order to reassemble the frame. Also see col. 6, line 61-64).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 and Gaddis '501 as taught by Koehler'660 for the same reason stated in Claim 7 above.

Regarding claim 13, Gaddis '501 discloses the step of determining where a packet ends from the length indicator with the separator (see Gaddis '501 col. 10, line 1-40; note that when ATM cells arrive from the network, the microprocessor examines to ensure all ATM cells, that belong to an Ethernet frame, are received by utilizing the frame size and frame size counter. Once an entire Ethernet frame arrives, Ethernet controller reassembles the Ethernet frame from the segments. In order to reassemble Ethernet frame from the ATM cells, the controller must identify where the frame ends.).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 and Gaddis '501 as taught by Koehler'660 for the same reason stated in Claim 7 above.

Regarding claim 14, Gaddis '501 discloses the step of removing the packet length information with the separator (see Fig. 10, Fig. 5 Ethernet frame and ATM cell, and col. 10, line 31-58; note that each time a new ATM cells is arrived, the size field is updated, which means that the current size of the frame must be deleted first in order to be updated. Once all ATM cells that belong to an Ethernet frame arrive, an Ethernet frame is reconstructed which as shown in Fig, 5, an Ethernet frame without SIZE field. Thus, it is clear that the size field is deleted after reassembly process at the Ethernet Controller).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 and Gaddis '501 as taught by Koehler'660 for the same reason stated in Claim 7 above.

Regarding claim 15, Cisneros '926 discloses the step of sending fragments of the packets from cross connect switch to the port card (see FIG. 3A, De-multiplexer 330 of the Interface Module 210; see col. 16, line 26-48; note that various parts of the cells, from the cross connect plane, are received at the interface module 210.) Gaddis '501 discloses the step of sending fragments of the packets from the separator to the interface adaptor (see Fig. 3 Ethernet Controller 22 and Serial Interface Adaptor; Since Ethernet segments are received at Ethernet controller, the same segments must be transmitted from Ethernet Controller to the interface adaptor as well.) Koehler'660 discloses sending stripes of fragments of the packets as described above in claim 7.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 and Gaddis '501 as taught by Koehler'660 for the same reason stated in Claim 7 above.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros '926 and Gaddis '501 and Koehler'660, as applied to claims 7-15 above, and further in view of Jones (U.S. 6,078,595).

Regarding claim 16, the combined system of Cisneros '926, Gaddis '501 and Koehler'660 discloses the step of sending fragments of the packet to the port card as

described above in Claims 7-15 above. Moreover, Cisneros '926 discloses, as shown in Fig. 5, transmitting and receiving cells between the cross connect planes 550 and Input 260/output 270 Modules.

Neither Cisneros '926, Gaddis '501 nor Koehler'660 explicitly discloses the step of sending fragments of the packet in a same logical time with corresponding fragments of the packet from other fabrics (see Jones '595 Fig. 1 Switch Fabrics (SF) 32a and 32b, BITS 14, and Physical Ports 22; see col. 4, line 10-67; note that both switch fabrics are externally timed with BITS (Building Integrated Timing Source) as a primary timing reference. Thus, when transmitting/receiving segments/cells/frames between the switch fabrics to the physical port, it must be synchronized within same clock cycle as primary timing reference.)

However, this limitation is taught by Jones '595. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Cisneros '926, Gaddis '501 and Koehler'660, as taught by Jones '595 for the purpose of providing synchronous data transfer within the switch of the present invention, buffering of data communicated between the various switch elements is minimized, reducing system cost, reducing data transfer latency, and enabling alignment of data phase and frequency; see Jones '595 col. 3, line 3-9. The motivation being that by utilizing the reference clock during the transmission of segments/cells/frames, it can minimize the clock slips or timing jitters, which cause failures in the switch and the networks.

7. Claims 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros '926, Gaddis '501, Koehler'660 and Jones '595, as applied to claims 7-16 above, and further in view of Joffe '086.

Regarding claim 17, the combined system of Cisneros '926, Gaddis '501, Koehler'660 and Jones '595 discloses the step of storing the fragments of the packet in a memory of the memory controller as described in above claims 7-16.

Neither Cisneros '926, Gaddis '501, Koehler'660 nor Jones '595 explicitly discloses a memory which has a wide cache buffer structure in which multiple packets are put into one word (see Joffe '086 Fig. 5, Shared Memory 26, bits from multiple ports (B1, B2) (i.e. note that multiple ports transmit/receive multiple packets), and Words (W1-Wn); see col. 5, line 46-67; note that each bit from each port is responsible for a single bit position in each word stored in the shared memory. When plurality of packets arrives at a port, each bit is transferred and stored into each word at the shared memory (i.e. Bit 1 to Bit m storing in each W1 to Wn).

However, this limitation is taught by Joffe '086. Joffe '086's shared buffer memory has a functionality of storing bits from various packets into a single word.) Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Cisneros '926, Gaddis '501,Koehler'660 and Jones '595, as taught by Joffe '086, for the purpose of designing an improved architecture for providing multiple port access to store multiple packets to a shared memory; see Joffe '086 col. 3, line 1-3. The motivation being that by designing a shared memory buffer which stores each bit from plurality of packets into a single word, it can reduce extra space in the shared buffer memory.

Regarding claim 18, Gaddis '501 discloses the step of extracting the packet length information from the packet with the separator (see Gaddis '501 Fig. 9 and col. 10, line 1-40; note that when ATM cells arrive from the network, the microprocessor examines to ensure all ATM cells, that belong to an Ethernet frame, are received by utilizing the frame size and frame size counter. Ethernet Controller extracts/reads each segment from the memory in order to reassemble the frame. When the segment is extracted/read, the size is also extracted/read from the memory since the size field is in the header of the cells. Also see col. 6, line 61-64).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926, Gaddis '501, Koehler'660 and Jones '595 as taught by Joffe '086 for the same reason stated in Claim 17 above.

Regarding claim 19, Cisneros '926 disclose receiving the fragments of the packet from the fabrics with an unstriper of the port card (see FIG. 3A, De-multiplexer 330 of the Interface Module 210 is an "unstriper"; see col. 16, line 26-48; note that various parts of the cells from the cross connect plane are received at the de-multiplexer.) Koehler'660 discloses the stripes of fragments of the packet as described above in claim 7.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926, Gaddis '501, Koehler'660 and Jones '595 as taught by Joffe '086 for the same reason stated in Claim 17 above.

Regarding claim 20, Gaddis '501 discloses aggregator of each fabric the fragments of the packet as described above in claims 1-19. Furthermore, Cisneros '926 disclose the step of sending with a striper of the port card (see Cisneros '926 FIG. 3A, Multiplexer 320 of the Interface Module 210 is a "striper of the port card".) to each fabric the fragments of packets (see Cisneros '926 col. 15, line 44-65; note that incoming user packets/cells, from the network, are received at the multiplexer.) Koehler'660 discloses the stripes of fragments of the packet as described above in claim 7.

Note that Cisneros '926 teaches transmitting segments of user packet from the multiplexer (which is within the interface card) to the cross connect switch plane. Gaddis '501 teaches transmitting segments of frame from interface adaptor to the Ethernet Controller (which is within the ATM-Ethernet portal fabric). Thus, Cisneros '926's multiplexer of the interface unit can be used to transmit segments of user packet to Gaddis '501's Ethernet controller which is within the ATM-Ethernet portal fabric. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926, Gaddis '501, Koehler'660 and Jones '595 as taught by Joffe '086 for the same reason stated in Claim 17 above.

Regarding claim 21, Gaddis '501 discloses the separator sending fragments to the port card as described above in claims 6-20. Cisneros '926 disclose sending fragments from fabrics to an unstriper of the port card (see FIG. 3A, De-multiplexer 330 of the Interface

Module 210; see col. 16, line 26-48; note that various parts of the cells, from the cross connect plane, are received at the de-multiplexer.)

Note that Gaddis '501 teaches receiving segments of user packets from the Ethernet Controller to network interface. Cisneros '926 teaches receiving segments of user packets from the cross connect plans to the de-multiplexer (which is within the interface card). Thus, Gaddis '501's Ethernet controller can be used to transmit the segments of the user packets to Cisneros '926's de-multiplexer which is within the interface card. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926, Gaddis '501, Koehler'660 and Jones '595 as taught by Joffe '086 for the same reason stated in Claim 17 above.

Notes/Remark

8. Drawing and specification objections are withdrawn since they are being amended accordingly.
9. Claim rejection under 35 USC 112, 2nd paragraph, on claim 20 is withdrawn since the claim is being amended accordingly.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 703-605-1531. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on 703-308-7828. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM
3/4/04

KENNETH VANDERPUYE
PRIMARY EXAMINER